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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,596	12/31/2001	Howard S. David	42390.P13873	2205

8791 7590 11/30/2006

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 11/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,596	DAVID, HOWARD S.	
	Examiner	Art Unit	
	Zhuo H. Li	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9,11,12 and 16-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9, 11-12, 16-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in responds to the Amendment filed on 10/24/2006.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 23 is rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (US PAT. 6,477,621 hereinafter Lee).

Regarding claim 23, Lee discloses a system memory (1009, figure 5) comprising at least two memory modules (300a through 300n, figure 5), each memory modules including at least one memory device (301-304, figure 3) and a data cache (601, figure 3) coupled to an eviction buffer (701, figure 3), both coupled to the memory device (col. 8 lines 7-42).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 20-22 and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (US PAT. 6,477,621 hereinafter Lee) in view of Akkary et al. (US PAT. 5,526,510 hereinafter Akkary).

Regarding claim 20, Lee discloses a memory module (300, figure 3) comprising at least one memory device (301-304, figure 3) and a data cache (601, figure 3) coupled to an eviction buffer (701, figure 3), both coupled to the memory device (col. 8 lines 7-42), the data cache controlled by a plurality of commands, i.e., read or write command, delivered by an external memory master, i.e., a memory controller, over a bus, i.e., a memory system interface (314, figure 3 and col. 9 line 48 through col. 10 line 20). Lee differs from the claimed invention in not specifically teaching the memory module to receive a write back command, the write back command to cause a previous line of data, evicted from the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the memory device. However, Akkary teaches in a data cache system comprising a plurality of cache banks (318, figure 2) and a write back buffer (322, figure 2) both coupled to the system memory via a system bus (308, figure 2) to perform memory operation in responds to an instruction from a central processing unit, wherein the write back buffer is capable of temporary storing the eviction entry from the cache bank, and further write back to a main memory such that a pervious line of data evicted from the data cache, which stored within the write back buffer, is written out of the write back buffer to the main memory (col. 6 lines 11-20 and lines 34-67). Therefore, it would have been obvious to a

person of ordinary skill in the art at the time the invention was made to modify Lee in having the memory module to receive a write back command, the write back command to cause a previous line of data, evicted from the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the memory device, as per teaching of Akkary, because it avoids coherency problems and performs replace operation more quicker.

Regarding claim 21, Akkary teaches the data cache to evict previous line of adapt the data cache into the eviction buffer according to an eviction signal received from the memory controller (col. 6 lines 12-20 and col. 6 line 34 through col. 8 line 27).

Regarding claims 24-25, Lee differs from the claimed invention in not specifically teaching a memory module to receive a write back command, the write back command to cause a previous line of data, evicted from the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the memory device of the memory module and wherein the memory stores a current line of data within the data cache of the memory module. However, Akkary teaches in a data cache system comprising a plurality of cache banks (318, figure 2) and a write back buffer (322, figure 2) both coupled to the system memory via a system bus (308, figure 2) to perform memory operation in responds to an instruction from a central processing unit, wherein the write back buffer is capable of temporary storing the eviction entry from the cache bank, and further write back to a main memory such that a pervious line of data evicted from the data cache, which stored within the write back buffer, is written out of the write back buffer to the main memory (col. 6 lines 11-20 and lines 34-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Lee in having the memory module to receive a write back command, the write back command to

cause a previous line of data, evicted from the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the memory device of the memory module and wherein the memory stores a current line of data within the data cache of the memory module, as per teaching of Akkary, because it avoids coherency problems and performs replace operation more quicker.

6. Claims 9, 11-12 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stracovsky et al. (US PAT. 6,378,049 hereinafter Stracovsky) in view of Lee et al. (US PAT. 6,477,621 hereinafter Lee) and Akkary et al. (US PAT. 5,526,510 hereinafter Akkary).

Regarding claim 9, Stracovsky discloses a system (100, figure 1B) comprising a processor (102, figure 1B), a memory controller (104, figure 1B) coupled to the processor, the memory controller including an array of tag address storage locations (114, figure 1B) and a command sequencer and serializer unit (116, figure 1B) coupled to the array of tag address storage locations, and a system memory (108, figure 1B) coupled to the memory controller (col. 6 lines 17-45). Stracovsky differs from the claimed invention in not specifically teaching the system memory including at least two memory modules, each memory module including at least one memory device and a data cache coupled to an eviction buffer, both coupled to the memory device, and the data cache controlled by a plurality of commands delivered by the memory controller. However, Lee teaches a system memory (1009, figure 5) comprising at least two memory modules (300a through 300n, figure 5), each memory modules including at least one memory device (301-304, figure 3) and a data cache (601, figure 3) coupled to an eviction buffer (701, figure 3), both coupled to the memory device (col. 8 lines 7-42), and the data cache

controlled by a plurality of commands, i.e., read or write command, delivered by an external memory master, i.e., a memory controller, over a bus, i.e., a memory system interface (314, figure 3 and col. 9 line 48 through col. 10 line 20) in order to flexibly serve different memory masters as required by data processing system to which the memory system is connected (col. 3 lines 24-35). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Stracovsky in having the system memory including at least two memory modules, each memory module including at least one memory device and a data cache coupled to an eviction buffer, both coupled to the memory device, and the data cache controlled by a plurality of commands delivered by the memory controller, as per teaching of Lee, because it flexibly serves different memory masters as required by data processing system to which the memory system is connected. Furthermore, neither Stracovsky nor Lee specifically discloses the memory controller writing a current line of data to the data cache and the memory controller to further instruct the data cache to evict a previous cache line of data cache into the eviction buffer. However, Akkary teaches in a data cache system comprising a plurality of cache banks (318, figure 2) and a write back buffer (322, figure 2) both coupled to the system memory via a system bus (308, figure 2) to perform memory operation in responds to an instruction from a central processing unit, wherein the write back buffer is capable of temporary storing the eviction entry from the cache bank, and further write back to a main memory such that a pervious line of data evicted from the data cache, which stored within the write back buffer, is written out of the write back buffer to the main memory (col. 6 lines 11-20 and lines 34-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Stracovsky and Lee in having the memory

controller writing a current line of data to the data cache and the memory controller to further instruct the data cache to evict a previous cache line of data cache into the eviction buffer, as per teaching of Akkary, because it avoids coherency problems and performs replace operation more quicker.

Regarding claim 11, Akkary discloses the memory controller to deliver a writeback command to the data cache, the writeback command to cause the previous line of data to be written out of the eviction buffer to the memory device (col. 6 lines 12-20 and col. 6 lines 34 through col. 8 line 27).

Regarding claim 12, Akkary discloses the writeback command including way information and bank address information (col. 7 line 48 through col. 8 line 16).

Regarding claim 16, Stracovsky discloses a memory controller (104, figure 1B) comprising an array of tag address storage locations (114, figure 1B) and a command sequencer and serializer unit (116, figure 1B) coupled to the array of tag address storage location, the command sequencer and serializer unit to control the system memory (col. 6 lines 17-45). Stracovsky differs from the claimed invention in not specifically teaching a data cache and an eviction buffer located on at least one memory module of the system memory. However, Lee teaches a data cache (601, figure 3) and an eviction buffer (701, figure 3) located on at least one memory module (300a through 300n, figure 5) of a system memory (1009, figure 5) in order to flexibly serve different memory masters as required by data processing system to which the memory system is connected (col. 3 lines 24-35). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Stracovsky in having the data cache and the eviction buffer located on at least one memory module of the

system memory, as per teaching of Lee, because it flexibly serves different memory masters as required by data processing system to which the memory system is connected. Furthermore, neither Stracovsky nor Lee specifically discloses the command sequencer and serializer unit to deliver a writeback command to the eviction buffer associated with memory module, the write back command to cause a previous line of data evicted from the data cache and stored within the eviction buffer, to be written out to the memory device of the memory module. However, Akkary teaches in a data cache system comprising a plurality of cache banks (318, figure 2) and a write back buffer (322, figure 2) both coupled to the system memory via a system bus (308, figure 2) to perform memory operation in responds to an instruction from a central processing unit, wherein the write back buffer is capable of temporary storing the eviction entry from the cache bank, and further write back to a main memory such that a pervious line of data evicted from the data cache, which stored within the write back buffer, is written out of the write back buffer to the main memory (col. 6 lines 11-20 and lines 34-67). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Stracovsky and Lee in having the command sequencer and serializer unit to deliver a writeback command to the eviction buffer associated with memory module, the write back command to cause a previous line of data evicted from the data cache and stored within the eviction buffer, to be written out to the memory device of the memory module, as per teaching of Akkary, because it avoids coherency problems and performs replace operation more quicker.

Regarding claims 17-18, Akkary discloses the memory controller issuing an eviction signal to the data cache to evict the previous line of data from the data cache into the eviction buffer, and also issuing the writeback command cause the previous line of data to be written out

of the eviction buffer to the memory device once the memory device is idle (col. 6 lines 12-20 and col. 6 lines 34 through col. 8 line 27).

Regarding claim 19, Akkary teaches a processor to cause a current line of data to be written from the processor (318, figure 2) to the data cache (318, figure 2) via fill buffer (320, figure 2), the processor to cause the previous line of data to be evict out of the data cache to the eviction buffer, i.e., writeback buffer (322, figure 2 and col. 6 line 12 through col. 8 line 27).

Response to Arguments

7. Applicant's arguments filed 10/24/2006 have been fully considered but they are not persuasive.

In response to applicant's terminal disclaimer over claims 1-21 of US Patent 6,925,534, the obviousness type double patenting rejection of claims 9, 11-12 and 16-25 are withdrawn.

In response to applicant's argument that Lee fails to show each and every element recited by claim 23, Examiner respectfully disagreed because Lee clearly discloses a system memory (1009, figure 5 and col. 15 lines 8-10) comprising a plurality of parallel connected memory systems (300-300n, figure 5, read as memory modules), wherein each memory module (300, figure 3) includes at least one memory device, i.e., a memory bank (301, figure 3) and a data cache, i.e., channel row cache memory (601, figure 3) coupled to an eviction buffer, i.e., cache row address register (701, figure 3) both coupled to the memory device. Note the broad claimed language of claim 23 fails to clearly define memory modules, as well as eviction buffers. Thus, Lee anticipates the broad claimed language as cited in claim 23 because Lee includes the presence of each and every element recited by claim 23.

In response to applicant's argument that the combination of Lee in view of Akkary fails to teach or suggest a memory module including at least one memory device, which is coupled to both a data cache and an eviction buffer, it is noted that Lee clearly teaches the above limitations (see previous paragraph) and the utilizing of Akkary is for teaching the memory module to receive a write back command, the write back command to cause a previous line of data, evicted from the data cache and stored within the eviction buffers, to be written out of the eviction buffer to the memory device (ass Akkary col. 6 lines 11-20 and lines 34-67). Thus, the combination of Lee and Akkary teaches or suggests all claimed feature recited by claim 20, as required to establish *prima facie* obviousness. Note claims 21-22 and claims 24-25, based on their dependency from claim 20 and 23, respectively, are also rejected under the combination of Lee and Akkary as the same reasons as set forth in above.

In response to applicant's argument that the combination of Stracovsky, Lee and Akkary fails to teach or suggest a memory module including at least one memory device coupled to both a data cache and an eviction buffers as recited in claim 9, it is noted that Lee clearly teaches the above limitations (see previous paragraph), which the utilizing of Stracovsky is for teaching a system comprising a processor, a memory controller coupled to the processor, the memory controller including an array of tag address storage locations and a command sequencer and serializer unit coupled to the array of tag address storage location (see Stracovsky col. 6 lines 17-45) and the utilizing of Akkary is for teaching the memory module to receive a write back command, the write back command to cause a previous line of data, evicted from the data cache and stored within the eviction buffers, to be written out of the eviction buffer to the memory device (ass Akkary col. 6 lines 11-20 and lines 34-67). Thus, the combination of Stracovsky, Lee

and Akkary teaches or suggests all claimed feature recited by claim 9, as well as claim 16. Note applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). As a result, examiner respectfully submits that the prior art combination of Stracovsky, Lee and Akkary teaches or suggests all claimed limitations recited by claims 9 and 16.

In response to applicant's argument that examiner has incorrectly interpreted cache row address register 701 as an eviction buffer, it is noted that examiner only interpreted cache row address register 701 as an eviction buffer for claim 23 because claim 23 fails to clearly define the function of the eviction buffer such that any kind of register can be interpret as the eviction buffer. For claims 9, 16 and 20, examiner relies on the combination of Lee and Akkary or the combination of Stracovsky, Lee and Akkary to reject the claimed invention. The above rejection, as well as previous rejection, clearly pointed out that Lee or the combination of Stracovsky and Lee fails to specifically discloses the memory module receiving a write back command, the write back command to cause a previous line of data, evicted form the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the memory device. Note Akkary teaches a method to perform replace operation much quicker in a data cache system by utilizing a write back buffer, read as eviction buffer, to temporary store the eviction entry from the cache bank and further write back to a main memory in respond to an instruction from a central processing unit (see Akkary, col. 6 lines 11-20 and lines 34-67). Thus, the combination of Lee

and Akkary and the combination of Stracovsky, Lee and Akkary teaches all claimed limitations as recited in claims 9, 16 and 20. As a result, the rejection is maintained.

In addition, claims 10-11 and claims 17-19, based on their dependency from claim 9 and 16, respectively, are also rejected under the combination of Lee and Akkary as the same reasons as set forth in above.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 571-272-4183. The examiner can normally be reached on Tues - Fri 9:00am - 6:30pm and alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zhuo H. Li

Patent Examiner
November 22, 2006

HONG CHONG KIM
PRIMARY EXAMINER